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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,945	08/10/2000	Setsuo Nakajima	SEL 203	5934

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,945	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-28 and 30-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-28 and 30-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 26-28 and 30-42 are objected to because of the following informalities and/or defects:

Claims 26, 27, 28 and 30-34 each recite the subject matters that an edge of the second layer of the input terminal portion is coplanar with an edge of the first insulating layer; but the original disclosure lacks an adequate description on it, especially regarding which edge of the second layer of the input terminal portion is coplanar with which edge of the first insulating layer. Applicant's remarks filed on September 28, 2005 contend that support for such subject matters can be found in Figs. 4 A and 4B and on Pages 22-23 of the specification. However, what shown in Figs. 4A and 4B are only truncated drawings, in which the extension of the second layer (208) of the input terminal portion and that of the first insulating layer (205) are both truncated (see the commonly recognized truncation symbol "≈" on the right side of the drawings). As Figs. 4A and 4B show only one TFT or pixel cell, no real edges of the two layers are shown there on the right side. Furthermore, both of the left edge (a real edge) and the truncated edge (the right side edge of the "input terminal portion") of the second layer in the input terminal are above, instead of being coplanar with, the first insulating layer in the input terminal portion. No adequate description on such subject matters can be found on Pages 22-23 of the specification, either.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-34 and 39-42, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (US 5,825,449).

Shin discloses a semiconductor device (Figs. 1a-1f; also see col. 1, lines 34-67), comprising: a substrate (1; glass); a thin film transistor comprising a gate electrode (2), a first insulating layer over the gate electrode, a channel forming region in an amorphous semiconductor layer (4), and doped source and drain regions (5); a second interlayer insulating layer (9; nitride, inorganic); a pixel electrode (6); a storage capacitor wiring ("20" and/or "2D"); and, a source input terminal portion (a source pad, also see the top row pads 640 in Fig. 6) including a first layer (2A) comprising the same material as that of the gate electrode (2) and a second layer (6A) comprising the same material as that of the pixel electrode in contact with the first layer through a contact hole formed in the first insulating layer, wherein the gate electrode, the storage capacitor wiring layer and the first layer in the input terminal portion all have a tapered shape and are formed from a same conductive layer; and the storage capacitor wiring and a portion of the pixel electrode, with a portion of the first insulating layer disposed therebetween,

inherently form a storage capacitor. The device further comprises a source wiring (7; also see source wiring 610 in Fig. 6), wherein a portion of the wiring (7) is formed over the source region (left side of film 5) and another portion of the source (7) is formed on the second layer (6A) of the source input terminal portion. And, it is also noted that the second insulating layer (9) in Shin can be regarded as being naturally overlapping with the pixel electrode (6), as the second insulating layer (9) therein overlaps with at least a portion of the pixel electrode (6).

Shin does not expressly disclose that the width of the first layer (2A) in the input terminal can be substantially larger that the width of the contact hole through which the first and second layers (2A, 6A) in the input terminal form a contact.

However, as further evidenced in Shin (Figs. 3 and/or 5), one ordinary skill in the art would readily recognize that such relatively larger contact-hole width is commonly desirable for easing the alignment requirement between the contact hole and the underlying first layer (2A and/or 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Shin with the width of the contact hole being made relatively larger compared to that of the underlying first layer, per the further teachings of Shin, so that a device with eased alignment requirement for the contact opening would be obtained. And, with such a contact hole having a relatively larger width being formed in the above device of Shin, the second layer in the input terminal therein would be naturally have an edge portion in which at least a bottom surface (such as the bottom surface of the second layer similar to layer 6A, 6C or 6D in

the input terminal in Figs. 3 and/or 5 in Shin) would be naturally coplanar with a bottom surface in an edge portion of the first insulating layer (similar to the bottom surface of the first insulating layer 3 above the first layer 2A or 2 in the input terminal in Figs. 3 and/or 5 in Shin).

Regarding claims 39-42, although Shin does not expressly disclose that the device can be applied in one of the selected applications as recited in these claims, each of these recited application are art-known applications for an LCD device such as the one of Shin, in order to achieve better display performance with reduced size, as readily evidenced in the prior art such as Ikeda et al. (US 5,428,250; see col.1, lines 16-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor device of Shin and applied it to one of the art-known applications, so that a better display performance in the application with reduced size would be obtained.

Claims 26-28, 30 and 35-38, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Ikeda et al. ("Ikeda"; US 5,428,250).

The disclosure of Shin is discussed as applied to claim 31-34 and 39-42 above.

Although Shin does not expressly disclose that the storage wiring can be completely covered by the pixel electrode, one of ordinary skill in the art would readily recognize that the storage wiring can be completely covered by the pixel electrode for

enhancing the storage capacitance therebetween, as evidenced in Ikeda (see the capacitor line 6 and the pixel electrode 10 in Figs. 6-12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device of Shin with the storage wiring being completely covered by the pixel electrode, as taught in Ikeda, so that an LCD device with enhanced storage capacitance would be obtained.

Response to Arguments

Applicant's arguments regarding Shi filed on September 28, 2005, have been fully considered but they are not persuasive. Responses to these arguments have been fully incorporated into the claim objections and claim rejections set forth above in this office action.

Applicant's other arguments with respect to the above rejected claims have also been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
December 10, 2005

SHOUXIANG HU
PRIMARY EXAMINER